This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-92 (canceled).

93. (currently amended) A planar conductive material structure usable in manufacturing an interconnect for an integrated circuit comprising:

a substrate having a top portion that includes a surface portion and a cavity portion, wherein the cavity portion has at least a first cavity having a width of less than one micron and a second cavity having a width larger than 10 microns; and

a planar conductive layer that is formed within the cavity portion and on the surface portion such that a predetermined thickness range of the planar conductive layer over the surface portion is between one tenth and one half of the thickness of the planar conductive layer within the cavity portion.

94. (canceled) ~~The structure of claim 93, wherein the first cavity has a width less than one micron, and the second cavity has a width larger than 10 microns.~~

95. (previously added) The structure of claim 93, wherein the top portion includes an insulator layer and a barrier layer overlying said insulator layer and wherein the cavities are formed in the insulator layer.

96. (previously added) The structure of claim 93, wherein the planar conductive material comprises copper or copper alloy.

97. (withdrawn)

98. (withdrawn)

99. (withdrawn)

100. (previously added) An integrated circuit including the structure of claim 93.

101. (previously added) The structure of claim 93, wherein the planar conductive material comprises copper.